WHAT IS CLAIMED IS:

1. A method for a wafer level chip scale package (CSP), the method comprising:

providing a semiconductor wafer, the semiconductor wafer including semiconductor chips having chip pads and a passivation layer, the wafer further including scribe lines between the chips;

forming a first patterned dielectric layer on the passivation layer to expose the chip pads; and

forming a second patterned dielectric layer on the first patterned dielectric layer to expose the chip pads,

wherein the second patterned dielectric layer has an embossed portion where a ball pad is to be formed.

2. The method of claim 1, wherein the embossed portion has a concave portion and a convex portion, the concave portion exposing a portion of the first patterned dielectric layer, the convex portion being formed of the second patterned dielectric layer.

3. The method of claim 2, wherein the concave portion comprises a circle shape, and the convex portion comprises a ring shape and having a smaller diameter than the concave portion.

4. The method of claim 2, wherein the convex portion comprises a discontinuous ring shape.

5. The method of claim 2, wherein the area of the concave portion inside the convex portion is approximately equal to the area of the convex portion.

6. The method of claim 1, further comprising:

forming a metal wiring layer on the first and second patterned dielectric layers including the embossed portion, the metal wiring layer being electrically connected to the chip pads;

forming a third dielectric layer on the metal wiring layer; and

removing a portion of the third dielectric layer over the embossed portion to form a connection hole therein, the connection hole exposing a portion of the metal wiring layer to form the ball pad.

7. The method of claim 6, further comprising:

forming a solder ball on the ball pad; and

cutting the semiconductor wafer along the scribe lines.

8. The method of claim 3, wherein forming a first patterned dielectric layer comprises exposing a portion of the passivation layer inside the ring-shaped second dielectric layer.

9. The method of claim 8, wherein forming a second patterned dielectric layer comprises exposing a portion of the passivation layer inside the ring-shaped second dielectric layer.

10. A method for a wafer level chip scale package (CSP) comprising:

providing a semiconductor wafer, the semiconductor wafer including semiconductor chips each having chip pads and a passivation layer;

forming a first dielectric layer on the passivation layer;

patterning the first dielectric layer to expose the chip pads;

forming a second dielectric layer on the patterned first dielectric layer; and

patterning the second dielectric layer to expose the chip pads,

wherein the first and second patterned dielectric layers form a ball pad area, in which the second patterned dielectric layer has a non-planar surface.

11. The method of claim 10, further comprising:

forming a metal wiring layer on the first and second patterned dielectric layers, the metal wiring layer being electrically connected to the chip pads;

forming a third dielectric layer on the metal wiring layer; and

removing a portion of the third dielectric layer over the non-planar surface to form a connection hole therein, the connection hole exposing a portion of the metal wiring layer over the non-planar surface to form a ball pad.

12. The method of claim 11, further comprising:

forming a solder ball on the ball pad.

13. A wafer level chip scale package (CSP), comprising:

a semiconductor chip having chip pads and a passivation layer exposing chip pads;

a first patterned dielectric layer disposed on the passivation layer; and

a second patterned dielectric layer, the first and second patterned dielectric layers exposing the chip pads,

wherein the first and second patterned dielectric layers have an embossed portion comprising a concave portion and a convex portion, the concave portion exposing a portion of the first patterned dielectric layer where a ball pad is to be formed, the convex portion being formed of the second patterned dielectric layer.

14. The apparatus of claim 13, wherein the concave portion comprises a circle shape, and the convex portion comprises a ring shape and having a smaller diameter than the concave portion.

15. The apparatus of claim 13, wherein the convex portion comprises a discontinuous ring shape.

16. The apparatus of claim 13, wherein the area of the concave portion inside the convex portion is approximately equal to the area of the convex portion.

17. The method of making the wafer level chip scale package (CSP) of claim 13, the method comprising:

providing a semiconductor wafer, the semiconductor wafer including a semiconductor chip having chip pads and a passivation layer, the wafer further including scribe lines between the chips;

forming a first patterned dielectric layer on the passivation layer to expose the chip pads; and

forming a second patterned dielectric layer on the first patterned dielectric layer to expose the chip pads, wherein the second patterned dielectric layer has an embossed portion where a ball pad is to be formed.